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(54) Volatile memory chip with non-volatile memory locations for storing quality information

(57) A volatile memory chip characterised in that it comprises a non-volatile memory location assembly in which information items concerning the quality of the chip are permanently stored, particularly relating to the speed distribution, the defect types, the defect topology, as well as the diffusion process of the particular chip.

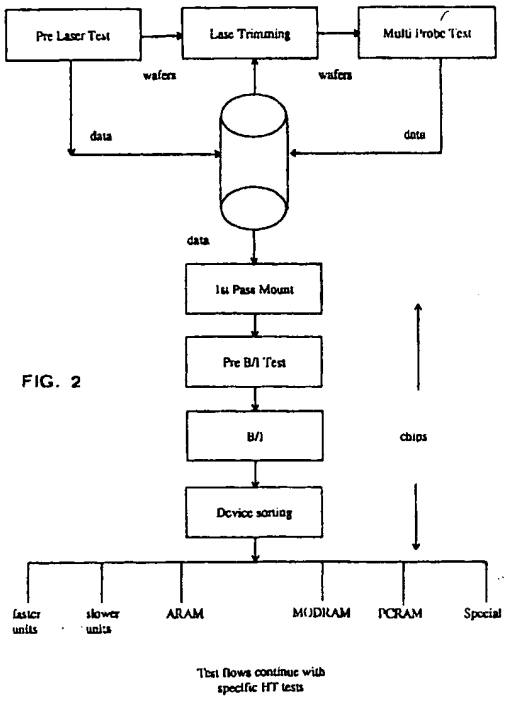

FIG. 2

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Description

FIELD OF THE INVENTION

The present invention broadly relates to semiconductor devices and more particularly concerns a memory device containing a non-volatile memory register, for permanently storing information pertaining to the quality of the device, particularly in connection with its speed and failure Figure, as well as in respect of a process for testing it.

BACKGROUND TO THE INVENTION

At present, the manufacture of semiconductor volatile memories, particularly silicon memories, includes three main stages: a chemical treatment stage for silicon, the test process for the devices as manufactured and the assembling stage of the devices satisfactorily tested.

At the end of the chemical treatment stage, very thin slices of silicon are obtained (known to those skilled in the art under the term *wafer),* usually having a substantially circular shape, subdivided into areas within which the individual memory devices are located (known under the term of *chips).* The assembly of the memory locations by which said individual chips are formed is organised into a matrix structure which in turn is subdivided into elements designated as sub-arrays, which include a constant number of said memory locations and are autonomously distinguished during the subsequent test stage.

The test process referred to above subjects the chips to a series of tests each of which checks the quality and/or the conformity of each individual chip to a predetermined design specification. The series of tests can be divided into two sets: a first set, that can be defined as the set of on-wafer tests and includes tests to be made on all of the chips of a wafer and a second set of tests, that can be defined as the set of the assembly tests that includes tests to be made on chips which have overcome the tests of the first set. The on-wafer tests enable information to be obtained concerning the failure Figures or rates, that is to say the failing sub-arrays. Furthermore, the speed of the chips is determined, on the base of which the failing chips are repaired by exploiting their redundancy, namely the sub-arrays realised in excess just to cope with this possibility. The tests of the first set are concluded by a test aimed at validating the result of the reparation operation. During these on-wafer tests, the maximum amount of information upon each individual chip of each individual wafer is collected in respect of the typology and the topology of the failures and to the speed level. The information, however, is stored upon computerised maps and is not utilised in the subsequent steps of the test program, because it is separated from the chips which it pertains to and therefore it is difficult and uncomfortable to be looked-up, so that it is virtually useless. This entails that the subsequent sequence of the assembly tests be divided into two distinct paths: a first path in which the quality of all those chips having positively overcome the on-wafer tests in order to sort them according to their speed level and a second path in which the quality of the so-called-Secondary Silicon, namely all those chips that have been found to be failing under a certain failure rate during the sequence of the on-wafer tests, in order to sort them according to the failure mechanisms occurring in the various circumstances. The separation of the assembly test flow makes it necessary to stock all those wafers containing even one only chip of Secondary Silicon until a number of lots sufficient to start the sorting tests of the Secondary Silicon is reached. In addition to the disadvantages associated with stocking of wafers with Secondary Silicon, the assembly test program requires that extremely complex tests be effected in order to obtain chip sorting information details that have already been obtained during the on-wafer tests. This entails a time expenditure that increases the manufacturing costs.

The assembly stage involving all those devices that have overcome the test program enables both the completely operative chips and the Secondary Silicon chips to be mounted for manufacturing memories of various typologies. In particular, it is possible to combine Secondary Silicon chips having compatible failure typology and topology. When it is desired to substitute any failing subarray with not-failing subarrays of other chips mounted in redundant number, a memory map is established in order to set up a correspondence between the logical addresses of the assembled memory and the physical addresses of the not-failing subarrays. When it is desired to establish said memory map, a further test sequence is to be carried out in order to operate the chips and to collect information relating to the failures found. The machines used to carry out said latter test sequence on the memory chips are complex and expensive and in addition, also in this case, all collected information details are the same as already obtained during the starting test sequence. This entails an increase in the manufacturing costs and reduces the speed of the. manufacturing process.

In conclusion, the manufacture of semiconductor , in particular silicon, volatile memories requires during the test and the assembly stages information concerning the failure rate as well as the speed of the chips. However, such information is only available on computerised maps, materially separated from the chips which it is related to, and, therefore, it is often fruitless because it is difficult and uncomfortable to be looked up. This means that this information must be repeatedly collected in different manufacturing stages, thereby increasing the manufacturing times and costs for said volatile memories.

SUMMARY OF THE INVENTION

The present invention provides a method for realising memory devices having permanently stored all information concerning their own failure rate and speed, so as to enable it to be looked up in any circumstance it is required by the various steps of the manufacturing process.

It is, therefore, specific subject-matter of this invention to realise semiconductor devices, particularly memory chips, containing a number of non-volatile locations, organised in one or more registers, in order to record information relating to the failure rates and to the speeds, as well as possibly to the diffusion process of the devices within which they are included.

An advantage of the memory location assembly according to this invention is that all information items concerning the failure rates and the speeds as well as the diffusion process of each individual chip type of each individual wafer are collected only once at the start of the test stage and they are easily and promptly read at the subsequent stages at any time the manufacturing step flow requires it.

In the preferred embodiment, the location assembly forms a register in which the information items are permanently stored by blowing out some fuses by a laser technique. Each bit or location of said register corresponds to a particular subarray of the chip and the information stored therein by blowing or maintaining the fuse pertains to the failure of the concerned subarray. Usually, 16 or 32 or 64 subarrays are included in a chip: consequently the register according to the invention has a size of 16 bits or 32 bits or 64 bits, such sizes being known to those skilled in the art as individual memory locations of 1 byte or of 1 word or of 1 nibble. Such register is accessed by means of a particular read operation not compatible with the conventional read/write operations of the concerned volatile memory. The particular read operation can be comprised of a specific voltage sequence applied to specific pins or the application of a voltage level higher than the levels utilised in conventional operation modes to the address pins. No further explanation is deemed necessary in this respect, since these read operations of particular information are already known and utilised and are perfectly known to those skilled in the art.

A variation of this embodiment could be based upon so-called Flash or EPROM memory locations. Further embodiments assume that an extended area of volatile memory and an area of a few Flash or EPROM memory locations be realised on the same chip.

Accordingly the present invention provides a method for testing memory devices, which method comprising; performing one or more tests for determining the functionality of memory elements in a plurality of main sub-arrays forming each memory device; storing data identifying each memory device in a register coupled to said memory device, such that data from the or each test can be associated with said memory device.

Preferably, the step of performing one or more tests comprises a Pre-Laser Test for obtaining data concerning failure rate and speed of each memory device. However, the tests may also include a Laser Trimming Test for repairing regions of the memory device determined to comprise a reduced functionality, and a Multi-probe Test for determining the result of repairing these regions.

Regions of the memory device which are found to have reduced functionality may be replaced by selecting a redundancy sub-array.

However, following the selection of the redundancy array, the tests for determining the functionality of memory elements must be repeated to ensure that the redundancy sub-array does not also have a reduced functionality.

Preferably address data identifying a main sub-array or a region of the main sub-array having reduced functionality is stored in the register. However, the register can also be used for tests performed for determining the cause of said reduced functionality.

Once the memory devices having reduced functionality have been identified they can be separated from the remaining memory devices.

Preferably all memory devices are subjected to a Pre-Burn-In Test which determines if memory devices having reduced functionality comprise a short-circuit or an open-circuit. However, to simplify the method, only those devices identified as having a reduced functionality may be subjected to the Pre-Burn-In-Test.

Preferably, all devices are subjected to a Burn-In Test in which the memory devices are operated under stressed environmental and operational conditions. This may comprise performing a read and/or a write cycle with the memory device and enables memory devices having reduced functionality to be identified.

Once testing has been completed the memory devices are sorted by typologies according to speed and operating characteristics determined in the tests. For example, memory devices that have reduced functionality may be used as ARAMS.

The memory devices can be sorted into various typologies according to speed and operating characteristics determined in the Pre-Laser Test, the Laser Trimming Test, or the Multi-Probe Test. Alternatively, the memory devices can be sorted into various typologies according to speed and operating characteristics determined in the Pre-Burn-In Test, or the Burn-In Test.

Accordingly, to a further aspects of the invention these is provided an apparatus for testing memory devices comprising; means for performing one or more tests for determining the functionality of memory elements in a plurality of main sub-arrays forming said memory device; means for communicating data for uniquely identifying each memory device to a register coupled to said memory device, such that data from the or each test can be associated with said memory device.

According to a yet further aspect of the present in-

vention there is provided a memory device comprising; a plurality of main sub-arrays forming said memory device; a register for storing data identifying said memory device, such that data from one or more tests performed on said memory device for determining the functionality of memory elements of the memory device can be associated therewith.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described by way of example with reference to the accompanying drawings in which:

Figure 1 shows a block diagram of a process performed during the test stage of the devices for manufacture of non-volatile memories,

Figure 2 shows a block diagram of a process performed during the test stage of devices provided with a register according to a preferred embodiment of the present invention for manufacture of volatile memories,

Figure 3 shows a device assembly diagram for manufacture of a non-volatile memory,

Figure 4 shows an electric wiring diagram for realising the correlation map between the logic addresses of the assembled memory and the physical addresses of the failure free subarrays,

Figure 5 shows an electric wiring diagram for realising the selection of a data line of a failure free subarray in substitution for a failure affected subarray.

DETAILED DESCRIPTION OF THE INVENTION

By referring now to Figure 1, it can be seen that the test program for devices obtained by means of the silicon chemical treatment process for manufacturing volatile memories subjects the chips to a test process which is subdivided into two sets: a first test set, the so called on-wafer tests, carried out on all chips of the wafers and a second test set, the assembly tests, carried out on all chips that overcome the first set tests.

The on-wafer tests begin with the so-called Pre Laser Test that enables information concerning the failure rate and the speed of the chips to be obtained. Based upon information concerning the failure rate, the subsequent Laser Trimming step performs the reparation of the failure affected chips by blowing out the fuses that enable utilisation of the redundancy, that is to say it enables substitution of the sub-arrays that have not overcome the Pre Laser Test with other failure free sub-arrays manufactured in excess on the chip just to cope with this possibility. The subsequent Multi Probe Test checks the results of the reparation operation. During the Pre Laser Test, the failure map for each chip of each wafer is stored in the computer in order to be reutilised during the Laser Trimming stage for determining the best reparation strategies; said failure map stored in the computer is defined as Wafer Map. However, said information items stored in the Wafer Map are no more utilised during the subsequent stages of the test program because they are physically separated from the chips they are related to and, therefore, they are difficult and uncomfortable to be looked up and are consequently dispersed. This entails that the subsequent sequence of the assembly tests be divided into two separate paths: a first path including a quality check on the chips having positively overcome the on-wafer tests based upon the speed level and a second path including a quality check on the Secondary Silicon , which is classified based upon the failure mechanism occurring therein.

During the set of the first test path of the assembly test, the Pre Burn-In Test, the Burn-In step , the High Temp. Test as well as the so-called Speed Sort are carried out, the latter test being designed to sort or to classify the chips based upon their speed level. This classification is performed by carrying out final tests positively designed to check whether the concerned chips match the specifications as established in connection with the various speed levels.

The Secondary Silicon chips are subjected to the test set of the second path of the assembly tests, during which the Pre Burn-In Test, the Burn-In step , the High Temp. Test as well as the so-called Device Sorting are carried out, the latter test being designed to sort or to classify the chips by identifying the device category which they to, based upon the failure typology. The classification is realised by carrying out final tests designed to check whether the concerned chips match the specifications as established in connection with the various device categories (such as ARAM MODRAM, PCRAM).

The procedures comprising the above mentioned assembly tests are well known to those skilled in the art and, therefore, further explanations in this respect are not considered necessary.

The separation of the assembly test flow into two distinct paths entails, as previously illustrated, the need to store all those wafers containing even a single chip of Secondary Silicon, so as to wait that a sufficient number of lots is reached to start the classification or sorting test for the Secondary Silicon. A further disadvantage of the presently employed manufacturing methodologies is the need for extremely complex tests to be executed in order to obtain sorting or classification information items of the chip, that have already been obtained, however, during the initial tests on the wafers. This entails an increase in the manufacturing times and costs.

During the assembly stage, the memory map is established based upon the topology of the failures on each individual chip and this is usually realised by suitably programming in permanent way an ASIC. To this purpose, some tests are to be carried out in order to establish the map of the failing subarrays within the chip. The procedure to carry out the tests and to program the above said ASIC turns out to be extremely complex,

time consuming and expensive.

Referring now to Figure 2, it can be observed that the exploitation of the register according to a preferred embodiment of the invention enables the test program to be unified into a single test flow designed to be carried out on all chips of the wafer, thereby avoiding to separate the assembly tests into a path including tests on completely operative chips and a path including tests on the Secondary silicon chips.

The set of on-wafer tests is very similar to the presently utilised one. The main difference to be observed is that, during the Laser Trimming stage, in addition to the fuse blowing operation aimed at repairing the chip, a fuse blowing operation aimed at storing any information concerning the failing subarrays of the chips is also performed. This means that the storage of the Wafer Map into the computer, even if it is illustrated in Figure 2, is not strictly necessary.

The subsequent set of assembly tests enables checking the quality both of the chips that have successfully overcome the on-wafer tests and of the Secondary Silicon chips, thereby maintaining a single manufacture lot up to the final test, specifically associated with each chip sorting class.

The following operations are carried out during the set of assembly tests:

- a 1st Pass Mount operation, in which the selection of the failure-free chips is performed,
- a Pre Burn-In Test operation, in which the chips are tested in order to locate any short-circuit or open-circuit condition,
- a Burn-In operation, in which the chips, upon being mounted on boards, are operated under stressed temperature and voltage conditions (125 °C and 78 volts) in write/read cycles, so as to eliminate all those chips that are found not to be adapted to withstand such conditions, and
- a sorting operation for the chips into the various typologies, so as to classify the chips by identifying the category they belong to, based upon their speed and failure grade. The classification is realised in simple and speedy way, because it is sufficient to carry out a read operation of the registers, that is to say a read operation of a single memory location. Only after this operation, does the test program flow separate the various chips based upon the information included in the registers, in order to carry out the final tests positively designed to check whether the concerned chips are in compliance with the pre-established specifications connected with the various device categories (such as speedy chips, slow chips, ARAM, MODRAM, PCRAM).

An advantage that is obtained by exploiting a register is observed in the noticeable simplification of the manufacturing process, in which it is no more necessary to stock the Secondary Silicon chips and to have two separate manufacturing lots. A further advantage is to be observed in that the storage of information pieces concerning the failure rate and the speed of the chips within the register makes them always available for looking up in speedy and simple way, thereby reducing the times needed for execution of the test programs and consequently the manufacturing costs.

During the assembly stage, any information details concerning the failure rates of the chips as stored in the register are utilised to build up the memory map based upon the number and upon the topology of all failing subarrays in each individual component chip, by simply programming an ASIC. In fact, the information details enable the various chips to be classified based upon the number and possibly upon the topology of all failing subarrays. Such a classification only needs a simple read operation in the register, the read operation being performed in very speedy times since, as above already said, it is a read operation involving a single location. Based upon said classification, Secondary Silicon chips can be assembled upon said memory board, in such an amount as to be sufficient to substitute all failing subarrays with failure free subarrays of other chips mounted in redundant number upon the memory board. The programming operation of the ASIC can be carried out in two possible ways, both of which are simple and fast and, therefore, advantageous with respect to the current procedures. A first way provides for utilising a computer based system that, by performing a read operation in the registers, as furnished each of the chips assembled to form the memory board, combines them with one another and consequently programs the ASIC logic. The algorithm for programming the ASIC based upon the information contents of the registers is easy to be exploited and, therefore, it does not require a complex computer system, but, in contrast, it only requires a Personal Computer provided with an interface for connection to the concerned ASIC. A second way to program the ASIC, in view of the simplicity of the map generating algorithm, provides for implementing a microcontroller incorporated with the ASIC for performing the read operation of the registers, as provided upon the component chips assembled to form the memory board, and, consequently, for programming the ASIC logic.

In view of the above, an advantage that can be obtained during the assembly stage by applying the register is to be observed in the simplification of the ASIC programming process, so that it is no more necessary to replicate the tests in order to establish the topology of all failing subarrays incorporated upon each chip, but it is sufficient to carry out a read operation of the registers, as provided on each chip. This entails a significant reduction in the assembly times of the memories and consequently a reduction in the manufacturing costs. A further advantage is to be observed in that the extremely complex and expensive machines needed for execution of the test aimed at generating the memory map are no more necessary. This entails a further and significant re-

duction of the manufacturing costs.

By referring now to Figure 4, the result of the operation for generating the correlation map between the logic addresses of the assembled memory and the physical addresses of all failing subarrays will be hereinbelow described. The logic address generated by a device accessing to the memory, such as a CPU, is mapped into a physical address that, according to whether the subarray resident upon one of the basic chips, the physical address of which is identical to the logic one, is either operative or failing, selects either said subarray resident upon one of the basic chips or the substitution subarray resident upon one of the redundant chips. The memory map, by which the physical addresses of failure free subarrays are made correspond to the logic addresses of the assembled memory is stored in the ASIC in a so-called address transcoding table. In the binary word forming the physical address of a subarray, the higher order bits are used to select the subarray, while the lower order bits are used to select the individual memory locations within the subarray. This applies both to the physical row address and to the physical column address. Mapping of a logic address into the physical one is performed by applying to said address transcoding table the higher order bits of the concerned logic address and collecting from the output of said table the higher order bits of the physical address and a multiplexer selection signal. When the subarray resident upon one of the basic chips is operative, the physical address will match the logic address and the selection signal will enroute the address to the multiplexer input over the address bus of the basic memory; otherwise, the physical address will be different from the logic one and the selection signal will enroute the address to the multiplexer input over the address bus of the redundant memory, in order to gain access to the substitution subarray resident upon one of the redundant chips.

By referring now to Figure 5, all data busses of the subarrays resident upon redundant chips are connected, by means of tristate input/output stages, to the data bus of the device, such as a CPU, that accedes to the memory. The connection between the data bus of the subarray corresponding to the logic address and the data bus of said device is realised by means of a decoder, driven by a selection signal coming from the address transcoding table stored in the ASIC, which selects the input/output stage of said specific subarray..

A further advantage deriving from the application of the register according to this invention is to be observed in that some manufacturing architecture standards exist, such as for instance SinkLink and Rambus, wherein some registers are provided in the memory and are dedicated to include particular information items, such as the manufacturer code, the memory model, the sizes of the device, the access speed. A register could be inserted among those already provided dedicated registers, thereby originating a specialisation of the existing standards.

By summarising all above described, the introduction of a non-volatile memory register into a volatile memory chip in order to record information pieces concerning the failure rate and the speed of the chip into which it is inserted simplifies the test and the assembly stages of the manufacturing cycle for volatile memories and makes it possible to reduce the manufacturing times and costs.

The preferred embodiments of this invention have been described and a number of variations have been suggested hereinbefore, but it should expressly be understood that those skilled in the art can make other variations and changes, without so departing from the scope thereof.

Claims

1. A volatile memory chip characterised in that it comprises a non-volatile memory location assembly in which information items concerning the quality of the chip are permanently stored.

2. A memory chip according to claim 1, characterised in that said memory locations are organised in one or more registers accessible by means of read operations that are not compatible with the conventional read/write operations of non-volatile memories.

3. A memory chip according to claim 1 or 2, characterised in that said non-volatile memory locations are implemented by blowing fuses during the laser trimming stage or by means of Flash or EPROM memory locations.

4. A memory chip according to any one of claims 1 to 3, characterised in that said information items relate to the speed distribution, the defect types, the defect topology, as well as the diffusion process of the particular chip.

5. A test method for volatile memory chips comprising an assembly of non-volatile memory locations organised in one or more registers in which information items are permanently stored conceming the speed distribution, the defect types, the defect topology, as well as the diffusion process of the chips, comprising the initial steps of : Pre Laser Test, that enables information concerning the failure rate and the speed of the chips to be obtained; Laser Trimming, that performs the reparation of the chips by blowing fuses; and Multi probe Test, that checks the results of the reparation operation; characterised in that:

   - during the Laser Trimming operation, in addition to blowing the fuses aimed at repairing the

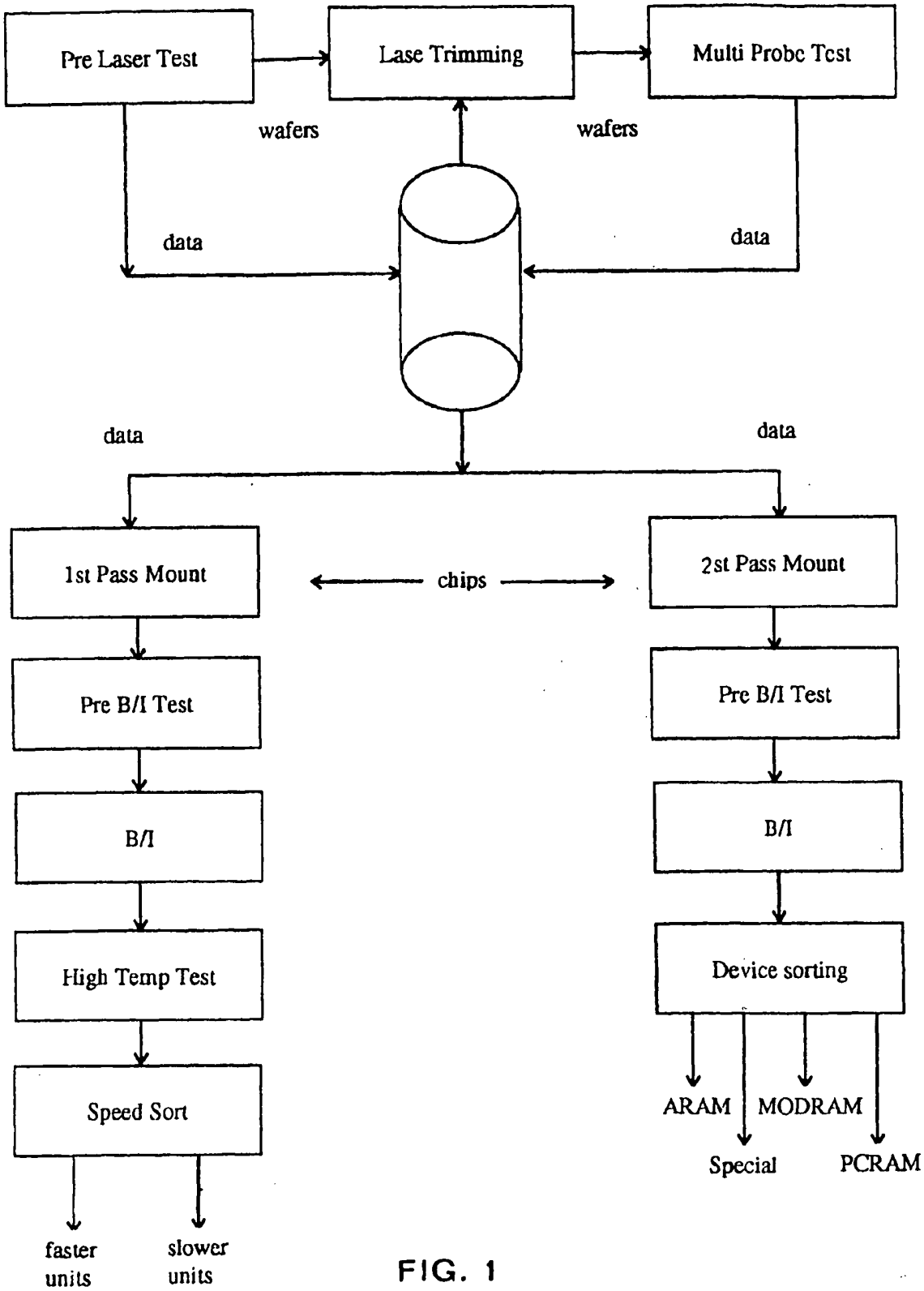
chips, a blowing operation is also carried out to blow fuses so as to store said information into the register;

and in that it further comprises the following set of operations carried out on the whole chip assembly to be tested:

- a 1st Pass Mount operation, in which the selection of the failure-free chips is performed,
- a Pre Burn-In Test operation, in which the chips are tested in order to locate any short-circuit or open-circuit condition,
- a Burn-In operation, in which the chips, upon being mounted on boards, are operated under stressed temperature and voltage conditions in write/read cycles, so as to eliminate all those chips that are found not to be adapted to withstand such conditions, and
- a sorting operation for the chips into the various typologies, according to their speed and operation characteristics.

6. A test method according to claim 5, characterised in that, before said final set of operations, a computerised compilation of a Wafer Map is carried out.

7. A memory chip including a non-volatile memory register for permanently storing information items concerning the product quality and related test method according to previous claims 1 - 4 and 5, respectively, and as previously described and shown in the enclosed drawings.


Pre Laser Test
Lase Trimming
Multi Probe Test
wafers
wafers
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chips
2st Pass Mount
Pre B/I Test
Pre B/I Test
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B/I
High Temp Test
Device sorting
Speed Sort
ARAM
MODRAM
Special
PCRAM
faster units
slower units

FIG. 1

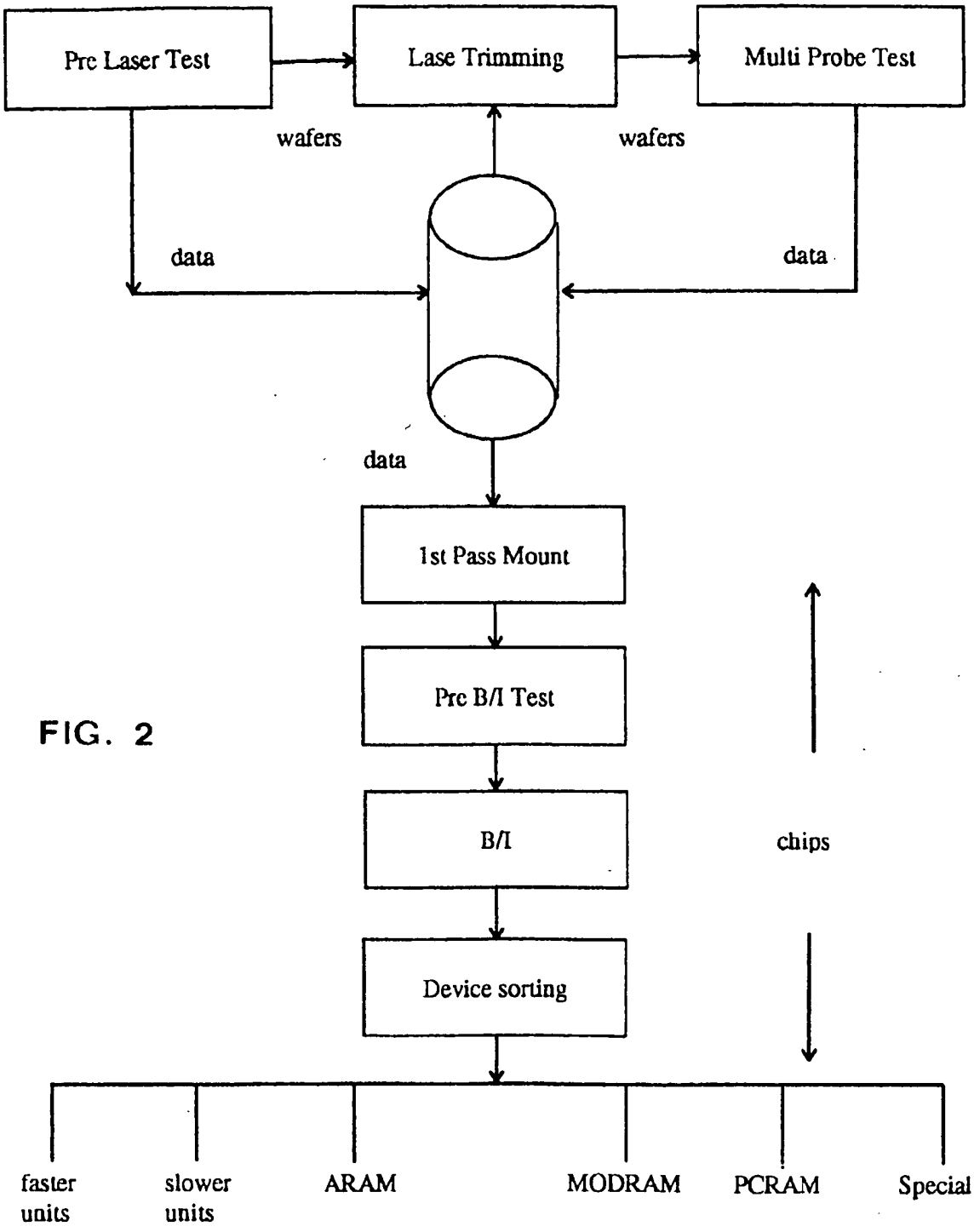

FIG. 2

Test flows continue with specific HT tests

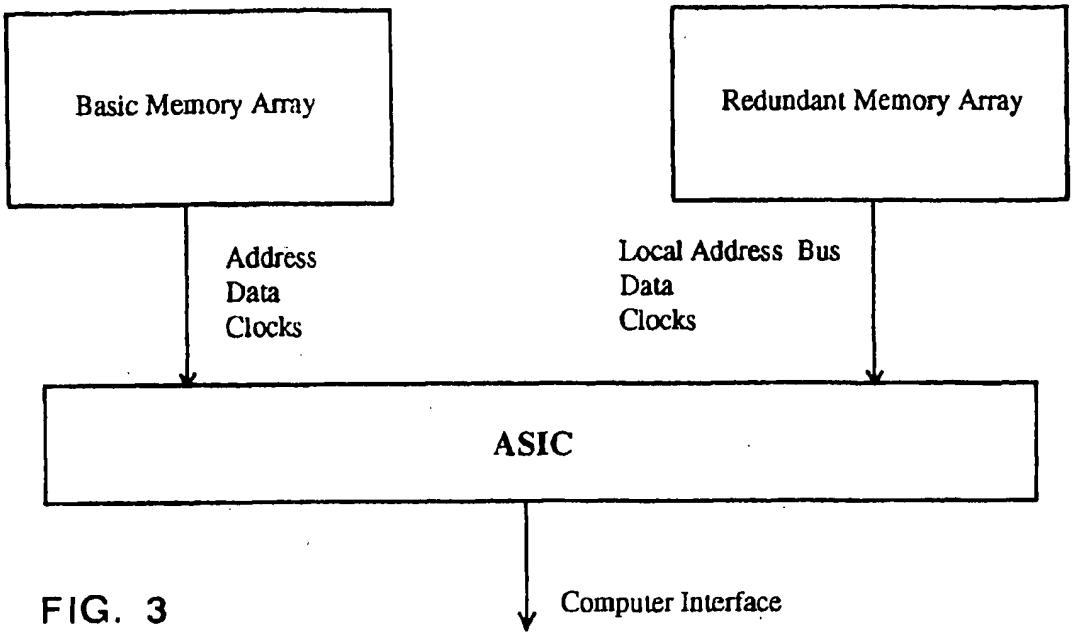
Basic Memory Array
Redundant Memory Array
Address
Data
Clocks
Local Address Bus
Data
Clocks
ASIC
Computer Interface

FIG. 3

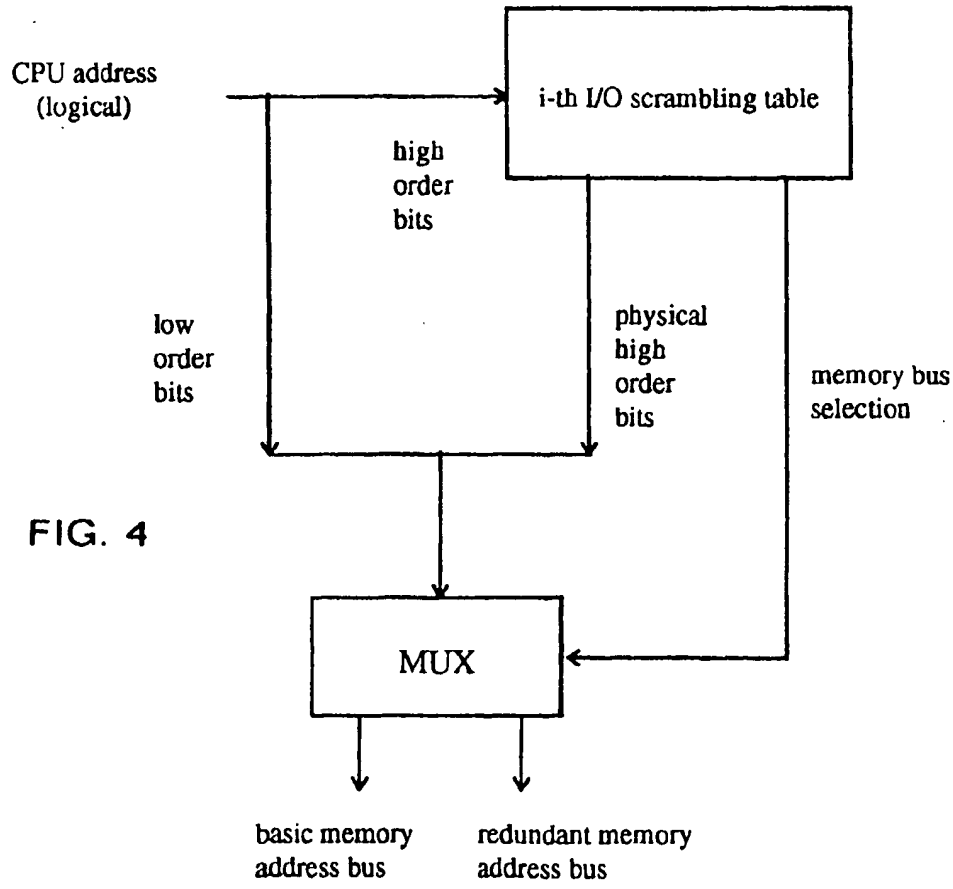
CPU address
(logical)
i-th I/O scrambling table
high
order
bits
low
order
bits
physical
high
order
bits
memory bus
selection
MUX
basic memory
address bus
redundant memory
address bus

FIG. 4

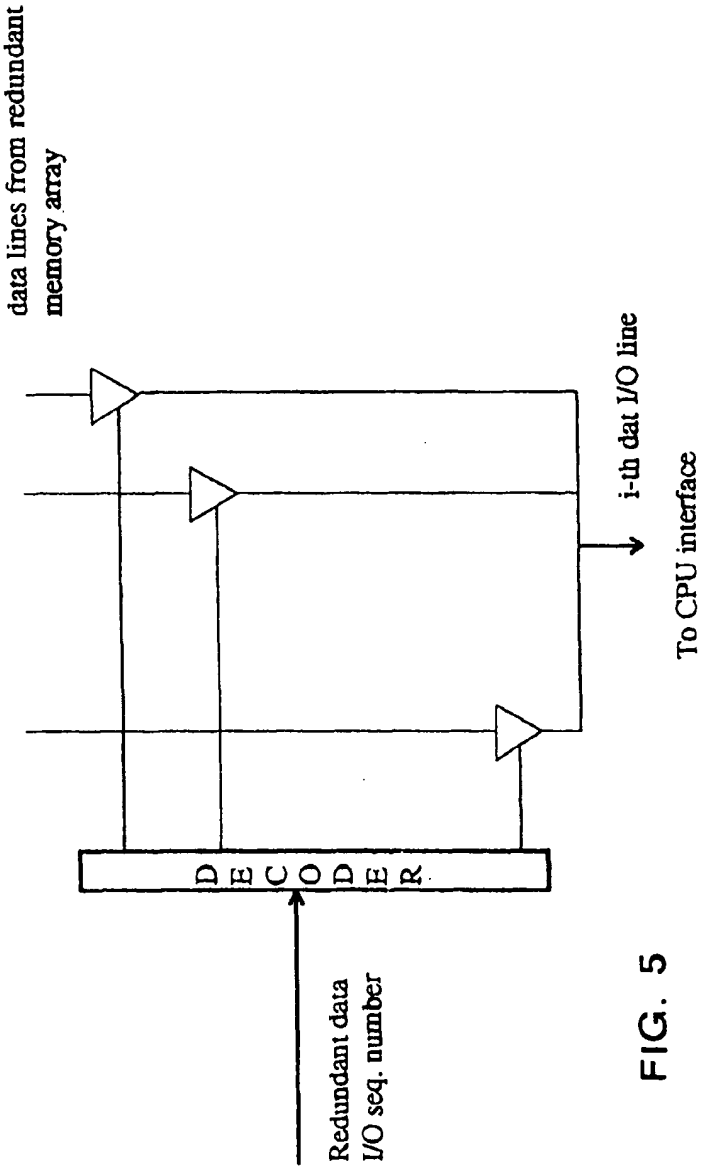

FIG. 5

TABLE 1

i-th I/O scrambling table				
	Physical row add	physical col add	redundant data I/O sequential number	redundant chip sequential number
Subarray #1				
Subarray #2				
=				
=				
Subarray #N				

DERWENT-ACC-NO: 1998-324920

DERWENT-WEEK: 200330

TITLE: Volatile memory chip with stored quality information - has non-volatile memory location assembly in which information regarding quality of chip are permanently stored

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BASIC-ABSTRACT:

The memory chip includes a non-volatile memory location assembly in which
information concerning the quality of the chip are permanently stored, particularly relating to the speed distribution, defect types, defect topology and the diffusion process of the particular chip.

USE - Permanently storing information relating to memory chip (e.g. FLASH

EEPROM) quality e.g. failure rate and speed, for retrieval if required during manufacturing process.

ADVANTAGE - All information concerning failure rates and speeds, together with
diffusion process of each chip on wafer are collected at start of test stage.

ABSTRACTED-PUB-NO: US 6130442A

EQUIVALENT-ABSTRACTS:

The memory chip includes a non-volatile memory location assembly in which
information concerning the quality of the chip are permanently stored, particularly relating to the speed distribution, defect types, defect topology and the diffusion process of the particular chip.

USE - Permanently storing information relating to memory chip (e.g. FLASH EEPROM) quality e.g. failure rate and speed, for retrieval if required during manufacturing process.

ADVANTAGE - All information concerning failure rates and speeds, together with
diffusion process of each chip on wafer are collected at start of test stage.

CHOSEN-DRAWING: Dwg.2/5

TITLE-TERMS: VOLATILE MEMORY CHIP STORAGE QUALITY INFORMATION NON VOLATILE
MEMORY LOCATE ASSEMBLE INFORMATION QUALITY CHIP PERMANENT STORAGE

DERWENT-CLASS: T01 U11 U13 U14

EPI-CODES: T01-G02; T01-G09; U11-C19A; U11-E02B3; U11-F01C3; U13-C04A1;
U13-C04B2; U14-A06B1; U14-D01A;

SECONDARY-ACC-NO:

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